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Energy Conversion Using Diode-Like Structures

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13.1 Introduction

A new type of device called a thermal diode is described.[1] It consists of a wafer of thermoelectric material and incorporates a carrier energy sorting potential barrier on the emitter side and an ohmic return current blocking barrier on the collector side. This device can be used for heat to electricity conversion or for cooling. Thermal to electric conversion with thermal diodes has been studied much more than cooling, so effort is focused primarily on this mode in what follows.

The first indication that potential barriers can improve the efficiency of PbTe thin films was reported in the 1970s.[2] There were subsequent theoretical and experimental attempts to use potential barriers in semiconductors[3–5] and on metal–semiconductor interfaces,[6] but high-efficiency devices have not materialized out of this work.

In experiments performed in our laboratory at ENECO in 2001, we observed significant enhancements of the open-circuit voltage and short-circuit current in a millimeter-scale semiconductor thermoelectric, on which a thin micron-scale emitter structure was added to the hot-side.[1] The resulting structure is indicated schematically in Figure 13.1. The addition of the emitter structure in these experiments would not have been expected to change the figure-of-merit significantly, but an enhancement of the integral figure-of-merit by as much as a factor of eight was measured.

According to our present understanding, the structure of the emitter for an n-type thermal diode is n^*pn, where n is the dopant concentration in the initial wafer (solid gap), p is a layer with p-type conductivity, and n^* is the electron source layer, that can be a metal or a heavily doped semiconductor. Our initial n^*n emitters,[1,8,9] when they worked properly, actually had a p-type layer due to a damaged region from wafer polishing. The collector had the same $n–p–n^*$ structure. Unlike the emitter, however, where p is a heavily doped layer, the collector layer doping can be close to intrinsic or compensated. A typical thickness of a wafer was approximately 1 mm, while typical thickness of emitter and collector barrier layers was around one micron. Barriers were formed by deposition, ion implantation or impurity

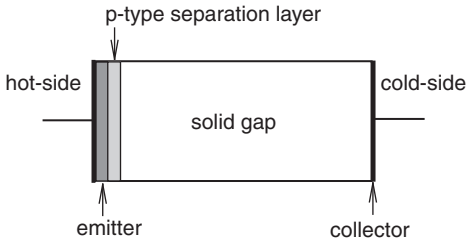

FIGURE 13.1 Schematic of a basic thermal diode. It includes a heavily doped emitter, p-type separation layer, and a near-intrinsic solid gap region. (*Source*: Hagelstein, P. and Kucherov, Y., Thermally induced current injection across an npn structure, *IEEE*, 2003. With permission.)

diffusion. Barriers were formed on the initial wafer and then samples were cut out of the wafer followed by testing of thermal and electrical parameters in a test apparatus.[1] Samples from the initial wafer without barriers produced thermoelectric currents and voltages consistent with the literature.

It might not have been expected that the addition of a thin emitter structure on a thick bulk thermoelectric could produce such a large enhancement in device efficiency. An analysis of the structure using a conventional thermoelectric description based on the Onsager current relation leads to the conclusion that either there should be no such effect, or else that new physical effects are involved. In the course of our research on this problem, we have come to think of the enhancement of the short-circuit current in terms of a second-order thermionic current injection. In this the forward-directed part of the electron distribution, that is out of equilibrium on one side of the barrier, does not balance the reverse-directed part of the distribution on the other side of the barrier. The enhancement of the open-circuit voltage is understood in terms of a voltage drop in the p-type separation layer needed to produce an ohmic electron return current to balance the forward-injected current. These effects are greatly enhanced under conditions where the mean-free path of the electrons is on the order of the barrier width.

13.2 InSb Thermal Diodes

InSb is a III–V semiconductor widely used in infrared sensing. An extensive properties database exists for this material in the literature. InSb is a mediocre thermoelectric with a maximum figure-of-merit $ZT \sim 0.2$. It has one of the highest mobilities among semiconductors and the largest scattering length near the room temperature.[12] It is also commercially available from multiple sources. As a result it is a good study material.

Initial wafers were typically doped with Te (n-type impurity) at $10^{18}\,\mathrm{cm}^{-3}$ concentration. Ion implanted or sputtered barriers were used on InSb.[10] Both kinds of barriers give approximately the same results for the same profiles and carrier concentrations. It is known[14,15] that a vacancy in InSb behaves as a p-type impurity with 50 meV ionization energy, which is well matched to the ionization energy of Te in InSb (50 meV with ⟨111⟩ orientation). Using inert gas ions, it is possible to induce an implantation profile with the required concentration of vacancies. Vacancy profile induced by ^{4}He implantation in InSb was calculated using TRIM code (IBM, 1991–1995). Corresponding potential barriers on the p–n interface were recalculated using Kane's model[11] and spin–orbit splitting parameter value $\Delta = 0.98$ eV from Ref. [15]. Fermi level shift as a function of ionized carrier concentration is shown in Figure 13.2.

The donors and acceptor concentration profile corresponding to the results below is shown in Figure 13.3. Negative concentration numbers on the *y*-axis correspond to n-type impurity.

Ion implantation gives better flexibility and control and was used for optimization of barrier height and thickness for deposition methods. We used a number of implantation doses corresponding to the anticipated position of the maximum performance peak. The implantation profile shape in all cases was the same as in Figure 13.3, but maximum concentration varied. Ion implanted wafers were cut into square samples with 1 to 2 mm sides. In–Ga contacts were used and electric output was measured in the

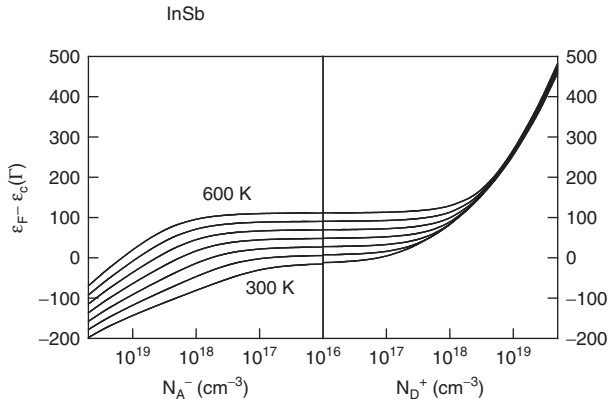

FIGURE 13.2 Fermi level shift in InSb as a function of ionized carrier concentration. (*Source*: Hagelstein P. and Kucherov, Y., Thermally induced current injection across an npn structure, *IEEE*, 2003. With permission.)

temperature range of 40 to 320°C. Experimental results in the form of open-circuit voltage in millivolts, short-circuit current density in amperes per square centimeter, and efficiency as a fraction of ideal Carnot cycle are shown in Figure 13.4.

The efficiency was calculated as a ratio of electric output to the heat flow through the sample. Relative efficiency (in terms of ideal Carnot cycle) of a thermoelectric sample (without implantation) was assumed to be unity and all results were normalized to these values. Ion implantation gave nearly a six times increase over baseline thermoelectric performance. The same results in the form of normalized electric output as a function of implantation dose (number of vacancies per volume unit) are shown in Figure 13.5.

Results of the measurements are shown in Figure 13.6 in the form of electric output normalized to thermoelectric behavior as a function of interface potential barrier height.

A large increase is observed with a barrier of 120 to 130 meV. This energy corresponds to the distance between the bottom of the conductivity band and the p-type impurity level ($E_g - E_i$). In our case the bandgap $E_g = 173$ meV and vacancy ionization energy $E_i = 50$ meV at room temperature. The peak follows bandgap and ionization energy temperature dependence. Higher barriers exhibit lower output. The peak stays $2k_BT$ wide at all temperatures.

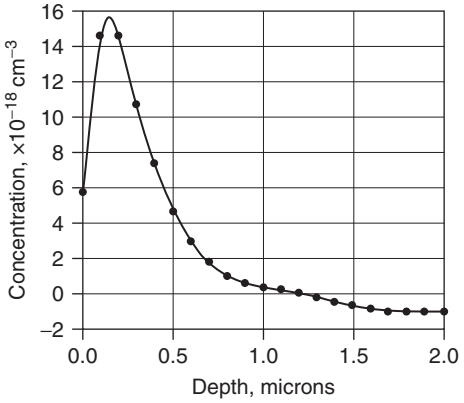

FIGURE 13.3 Dopant concentration profile after 4-He implantation. (*Source*: Hagelstein P. and Kucherov, Y., Thermally induced current injection across an npn structure, *IEEE*, 2003. With permission.)

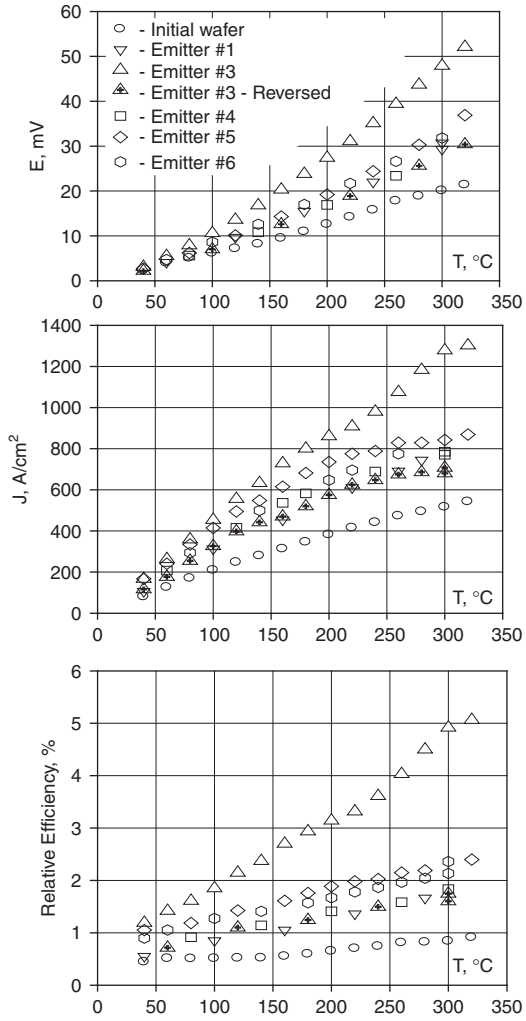

FIGURE 13.4 Open-circuit voltage, short-circuit current and relative efficiency for initial and ion implanted samples. (*Source*: Kucherov, Y., Hagelstein, P. et al., *IEEE*, 2003. With permission.)

When the sample was inverted, with the barrier on the cold-side and with the same thermal gradient, results were exactly the similar as in the Figure 13.4 for low temperature. In this case the gap region emitted into the cold contact. This result indicates that the dominant feature for the barrier effect is the junction temperature. In addition multiple junctions can be optimized to give extremely high efficiencies, which is consistent with earlier observations for thermal diode stacks.

Another optimization parameter is the potential barrier width. Numerical modeling of barrier structures[8] predicts no deviations from thermoelectric behavior when the barrier width is much greater than the majority carrier scattering length. The electron scattering length in intrinsic InSb is $\sim 0.8\ \mu$m.[13] Doping and ion implantation introduce scattering and recombination centers that reduce the scattering length. The degree of this reduction is not known for devices tested at this point. The contribution from recombination can be estimated in a three-level model[7] and gives a value of 10 to 15% at room temperature. Barrier widths were selected to be 0.4, 0.8, 1.5, and 3 μm. Modeling predicts a return to thermoelectric performance after five to ten scattering lengths or 4 to 8 μm of barrier width. We selected

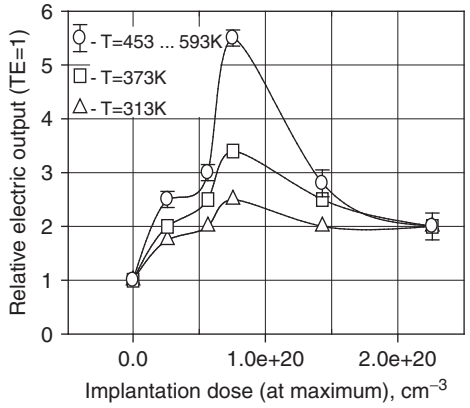

FIGURE 13.5 Electric output of InSb thermal diodes normalized to thermoelectric performance as a function of emitter implantation dose. (*Source*: Kucherov, Y., Hagelstein, P., et al., *IEEE*, 2003. With permission.)

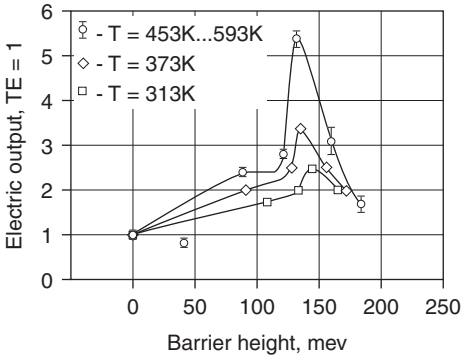

FIGURE 13.6 Electric output of InSb thermal diodes normalized to thermoelectric performance as a function of emitter barrier height. $T_{cold} = 290$ K. (*Source*: Kucherov, Y., Hagelstein, P., et al., *IEEE*, 2003. With permission.)

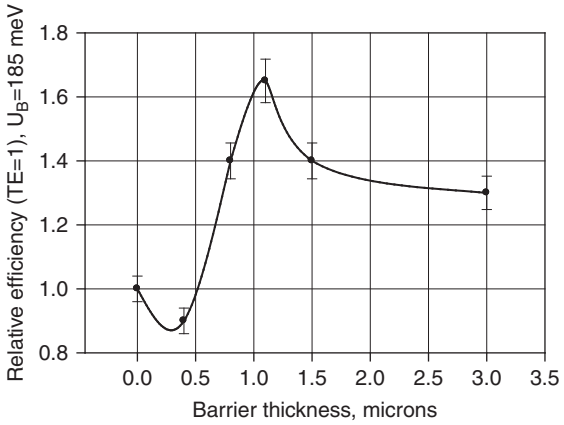

FIGURE 13.7 InSb thermal diodes electric output normalized to thermoelectric performance as a function of emitter barrier thickness. Barrier height is 185 meV. $T_{hot} = 573$ K; $T_{cold} = 290$ K. (*Source*: Kucherov, Y., Hagelstein, P., et al., *IEEE*, 2003. With permission.)

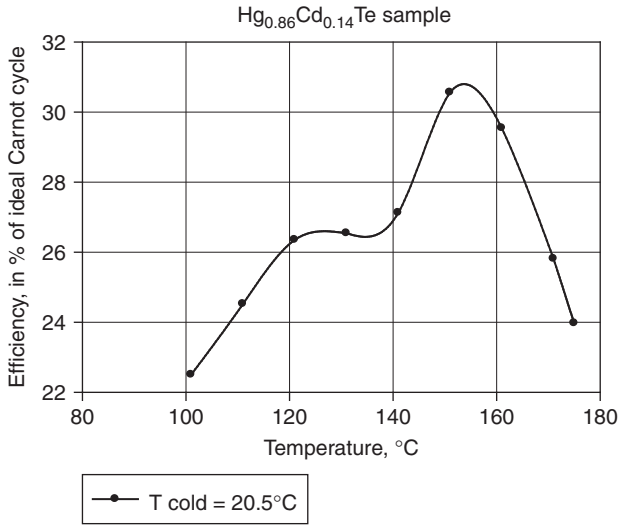

FIGURE 13.8 Efficiency (in percent of ideal Carnot cycle) for 0.5 mm thick intrinsic MCT sample ($x = 0.14$) as a function of a hot-side temperature. The cold-side was kept at 20.5°C.

a 185 meV barrier height for our parametric study. This barrier height is in the region where the efficiency dependence on concentration is mild and dose fluctuations are less important. Experimental results are shown in Figure 13.7.

In terms of thickness barrier structures behave according to modeling. Optimization of the barrier shape is of interest in future studies. For example, it is noted that a triangle-shaped barrier often outperforms a rectangular barrier.

13.3 HgCdTe Thermal Diodes

Mercury cadmium telluride (MCT), another material used in infrared sensing, is a better choice for thermal diode formation than InSb. Although its carrier mobility is lower, its figure-of-merit is double due to a much lower thermal conductivity. Another positive feature of MCT is the increase of a bandgap with temperature, which compensates for the barrier height decrease. The downside of this material is its instability at temperatures over 300°C when it starts to lose mercury unless some measures are taken to prevent the same. Physical properties of MCT are summarized in Ref. [16]. Barriers on MCT can be deposited by chemical vapor deposition, etc., but it is relatively expensive and direct diffusion is used to form a p-type layer. It is known[17] that diffusion of In into MCT displaces mercury and creates a p-type layer. We used In and InGa eutectic as a diffusing layer. MCT sample with deposited Cu contacts served as a thermoelectric reference. Efficiency measurement results for an intrinsic ($n = 10^{16}$ cm^{-3}) $Hg_{0.86}Cd_{0.14}Te$ ($x = 0.14$) thermal diode with 0.5 mm thickness are shown in Figure 13.8. Calculated maximum performance was expected at $x = 0.12$, but this composition had inclusions of semimetallic phase and $x = 0.14$ works better.

The efficiency is higher than for any thermoelectric converter and more than eight times higher than for thermoelectric reference with the same material. After 150°C the efficiency degrades due to diffusion in the emitter layer. Attempts to stabilize the same MCT composition by adding 10^{18} cm^{-3} of iron (electrically neutral) resulted in thermal diodes with 40% of ideal Carnot cycle efficiency at 280°C.[9,18]

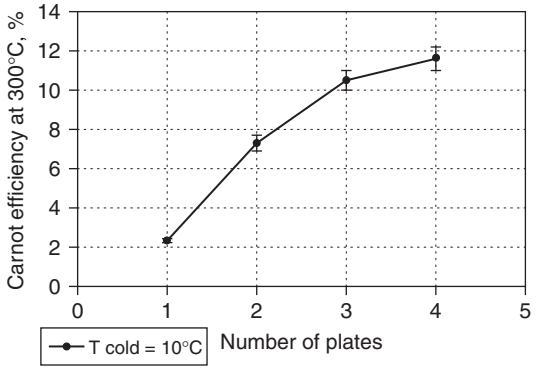

FIGURE 13.9 Efficiency of InSb thermal diode stacks in percent of ideal Carnot cycle at 300°C. Each thermal diode plate is 0.5 mm thick with 10^{18} cm^{-3} Te concentration in the gap. One-micron thick deposited emitter barrier with 25% gain over thermoelectric.

13.4 Multijunction Thermal Diodes

A multijunction approach is based on the fact that after five to ten scatterings after the first barrier, a carrier returns to non-perturbed Fermi distribution and the next barrier formed has the same effect as the first one. For a given temperature difference thermoelectric performance is a function of material properties. Barrier effects are additive and large gain in efficiency can be expected. An example of experimental study of thermal diode stacking, which is one of the ways to build multijunctions, is shown in Figure 13.9.

Plates of the same size were stacked one on top of another with InGa eutectic for thermal and electric contacts. The emitter in this case was of mediocre quality, giving only 25% gain over thermoelectric performance of the same material. Optimized thermoelectric performance for this material corresponds to ~8% of ideal Carnot cycle at the same temperature. With the increase of the number of plates, poor contact quality offsets gain from the barrier effect and the curve flattens.

Figure 13.10 shows the absolute efficiency of a stack made of InSb and MCT thermal diodes with separately measured absolute efficiencies at corresponding temperatures of 3.5% and 10%. Numbers for the stack were found to be higher than the sum of components. Measured open-circuit heat flow through the stack in this case is 50% lower than can be expected from the thermal conductivity of two plates. Temperature measurements with infrared camera for these kind of stacks show large temperature drops

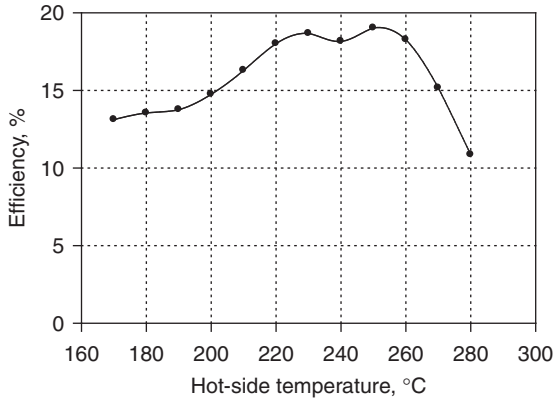

FIGURE 13.10 Absolute efficiency of InSb and MCT ($x = 0.14$) thermal diodes stack as a function of temperature.[18] Plates were 2 and 0.5 mm thick.

on the interfaces, which are an order of magnitude larger than what can be expected from contact thermal resistance.

In principle, the multiple barrier approach allows to achieve internal efficiencies approaching the ideal Carnot cycle with any semiconductor, provided that potential barriers can be built and interface quality is high. The number of barriers estimated for 90% device internal efficiency varies from only a few for efficient gap materials, like MCT, Cd_3As_2, PbTe, to $\sim$20 for InSb or to 200 for silicon.

13.5 Modeling Issues

The experimental results discussed above lead immediately to the conclusion that the approximations leading to the Onsager current relation

$$J = \sigma\left(\frac{1}{q}\nabla\varepsilon_{\mathrm{F}} - \Sigma\nabla T\right) \tag{13.1}$$

break down. As this relation can be developed directly from a linearization of the transport equation in the relaxation time approximation, it is natural to suspect that the carrier distributions have been driven sufficiently far from equilibrium in these devices that linearization is no longer a good approximation. The width of the junction in these experiments is of the order of the scattering length of a significant fraction of the electrons in these experiments, which supports the notion that nonequilibrium effects are involved. We expect that a full solution of the transport equation combined with the Poisson equation should be sufficient to account for the increased short-circuit current and open-circuit voltage, but this has not yet been attempted for this problem.

Instead an attempt has been made to understand the problem more simply in terms of somewhat idealized pictures. We consider first the case of the short-circuit current density, where the notion of a second-order thermionic current injection effect appears to be relevant. In an abrupt n^*n junction model, where an emitter is next to the solid gap (bulk semiconductor region), a region of high electron density exists on one side of the junction and a near intrinsic region on the other side. In thermal equilibrium, the forward current from the emitter balances the reverse current from the solid gap region, and no net current flows. If a thermal gradient is present, then it is found in a naïve calculation that assume no Fermi level discontinuity at the junction, that the forward current from the emitter is not balanced by the backward current from the solid gap region due to the part of the distribution on both sides that is not Fermi–Dirac. The net current injection in this simple model seems to be on the order of what is present in the experiments, both in the magnitude and in the observed proportionality to the thermoelectric current density. We have termed this mechanism a second-order thermionic current injection effect. An extension of this model to include scattering length effects and finite junction effects was found to give numerical results those were in good agreement with experiment with InSb thermal diodes.

It is possible to compute the open-circuit voltage with this model by assuming that an induced voltage was needed to provide a matching ohmic return current, with good results. Such a model does not shed light on how this might come about microscopically, and attempts to make the naïve current injection model outlined above predictive, leads quickly to the conclusion that there cannot be an enhancement in the open-circuit voltage over thermoelectric values by more than tens of microvolts in an n^*n junction. Any voltage drop in such a junction would be immediately shorted out. This argument led to the conclusion that there had to be a p-type blocking layer present in order to support a voltage drop, to be consistent qualitatively with the experimental measurements. Once this was understood, an examination of the devices which were most successful showed that such a p-type layer was present. Experiments that produced controlled p-type layers as discussed above clarified this issue.

These results have led to the development of a new transport model that appears to be relevant for this effect. The transport equation in the relaxation time approximation is given by

$$\left[\frac{1}{\hbar}\nabla_{\mathrm{k}}\varepsilon\right]\nabla f - \left[\frac{1}{\hbar}\nabla\varepsilon\right]\nabla_{\mathrm{k}} f = \frac{f_0 - f}{\tau_{\mathrm{s}}} \tag{13.2}$$

and then write a formal integral solution

$$f = \int e^{-\tau}[S_-(\tau)\Theta(k_z) + S_+(\tau)\Theta(-k_z)]d\tau \tag{13.3}$$

This kind of solution is similar to those employed in radiation transport problems, where τ is the optical depth along an electron trajectory, and S is the source function. If we approximate the local source function by the local Fermi–Dirac function

$$f_0 = \frac{1}{e^{(\varepsilon-\varepsilon_F)/k_BT} + 1} \tag{13.4}$$

it results in an approximation, which is nonlocal, and which should provide a better description than would be obtained from linearization. This estimate can then be used for the distribution to develop a nonlocal generalization of the Onsager current relation

$$J = -q\left\langle \nu(k)\int d\tau\, e^{-\tau}\left[\left(\frac{1}{e^{\frac{\varepsilon-\varepsilon_F}{kT}}+1}\right)_-\Theta(k_z) + \left(\frac{1}{e^{\frac{\varepsilon-\varepsilon_F}{kT}}+1}\right)_+\Theta(-k_z)\right]\right\rangle \tag{13.5}$$

This expression reduces to the Onsager relation in the limit that the scattering length is small. It also reproduces the second-order thermionic current injection estimate in the naïve current injection model mentioned above. In the case of an n^*pn emitter structure, it has been successfully verified that this model leads to an open-circuit voltage enhancement that is on the order of that which is experimentally observed.[19]

Exploratory calculations with this model indicate that the new effects are maximized when the electron scattering length is matched to a factor of roughly three drop in the electron concentration. If the p-type separator region is not thick enough, or the barrier is not large enough, then the open-circuit voltage is shorted out. If the barrier is too high and too thick, then the electron injection cannot go through the barrier, and the efficiency will be degraded. Hence there is expected to be optimum barrier width and height from theory which can be estimated readily. The experimental results appear to be consistent with this picture. When operating properly, the emitter structure acts in these models as an equivalent thermoelectric with an enormous effective thermopower resulting from these nonequilibrium transport effects. We have seen enhancements in the range of two to three orders of magnitude as compared to the solid gap region.

References

1. Hagelstein, P. and Kucherov, Y., In *Proceedings of the 2001 Fall MRS Conference*, G.S. Nolas, ed., Vol. 691, pp. 319–324. Boston, MA, 2001.
2. Gudkin, T.S., Drabkin, I.A., Kardanov, V.I., and Sterlyadkina, O.G., *Phys. Technol. Semicond.*, 8, 2233, 1974, (in Russian).
3. Ravich, Y.I., In *CRC Handbook of Thermoelectrics*, D.M.Rowe, ed., pp. 70–73. New York, 1995.
4. Moyzhes, B.Y., *Proceedings of the 15th International Conference on Thermoelectrics*, Pasadena, CA, pp. 183–187. 1996.
5. Shakouri, A. and Bowers, J.E., *Appl.Phys. Lett.*, 71, 1234, 1997.
6. Mahan, G.D. and Woods, L.M., *Phys. Rev. Lett.*, 80(18), 4016–4019, 1998.
7. Sze, S.M., *Physics of Semiconductor Devices*, 2nd ed. Wiley, New York, 1981.
8. Hagelstein, P. and Kucherov, Y., *Proceedings of the 21st International Conference on Thermoelectrics*, pp. 400–403, 2002.
9. Hagelstein, P.L. and Kucherov, Y., *Appl. Phys. Lett.*, 81(3), 559–561, 2002.
10. Kucherov, Y., Hagelstein, P., Sevastyanenko, V., and Brown, H.L., *Proceedings of the 22nd International Conference on Thermoelectrics*, pp. 578–581, 2003
11. Kane, E.O., *J. Phys. Chem. Solids*, 1, 249, 1957.

12. Madelung, O., *Physics of III–V Semiconductor Compounds*, Springer Verlag, Berlin, 1967.
13. Dubowski, J.J., Dietl, T., Szymanska, W., and Galazka, R.R., *J. Phys. Chem. Solids*, 42, 351, 1981.
14. Zaitov, F.A., Gorshkova, O.V., Polyakov, A.Ya., Kevorkov, M.N., and Popkov, A.N., *Sov. Phys. Semicond.*, 15(6), 711, 1981.
15. Landolt–Borstein, *Numerical Data and Functional Relationships in Science and Technology*, Springer, Berlin, 1982.
16. P. Capper, ed., *Properties of Narrow gap Cadmium-Based Compounds*, EMIS Datareviews Series No.10, INSPEC, 1994.
17. Margalit, S. and Nemirovsky, Y., *J. Electrochem. Soc.*, 127, 1406, 1980.
18. Kucherov, Y., Hagelstein, P., and Sevastyanenko, V., *Proceedings of the 21st International Conference on Thermoelectrics*, pp. 431–434, 2002.
19. Hagelstein, P. and Kucherov, Y., *Proceedings of the 22nd International Conference on Thermoelectrics*, pp. 554–557, 2003.